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Prototyping Feed-Forward Artificial Neural Network on Spartan 3S1000 FPGA for Blood Type Classification

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ABSTRACT

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Keywords Feed-Forward, Artificial, Neural-Network, FPGA, Xilinx, Spartan 3A, Blood type classification. In this research, a Feed-Forward Artificial Neural Network design was implemented on Xilinx Spartan 3S1000 Field Programable Gate Array using XSA-3S Board and prototyped blood type classification device. This research uses blood sample images as a system input. The system was built using VHSIC Hardware Description Language to describe the feed-forward propagation with a backpropagation neural network algorithm. We use three layers for the feed-forward ANN design with two hidden layers. The hidden layer designed has two neurons. In this study, the accuracy of detection obtained for four-type blood image resolutions results from 86%-92%, respectively.

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1. Introduction

Blood type is a distinctive feature that every person has. Identification of blood type is important in the case of blood transfusion. There are 4 blood types, i.e., A, B, AB, and O. In the world of medication, medical instances still use conventional ways of identifying blood types. The conventional way is achieved by dripping antiserum reagent to a blood sample. After that, conglomeration will occur, and the tester will have to compare the reagent-dripped sample with another sample with a different antiserum reagent in medical. In big-scale sample testing, this method will not be efficient as it takes a very long time and can cause dissatisfaction to the customers who wish to test their blood samples. Hence, automation of blood type identification is needed [1]-[3].

Using a Field Programmable Gate Array, an electronic and logical device can be designed and used anywhere and anytime with digital circuits. FPGAs have higher speed and smaller size for real-time application than the VLSI design. It also provides flexibility and yields the availability of fast special-purpose hardware for wide applications in programmable systems. For the neural network-based instrument prototype in a real-time application, conventional VLSI neural chip design suffers the limitation in time and cost. In addition, artificial neural network based on FPGAs has fairly achieved with classification application [4].

This research will involve implementing Artificial Neural Network (ANN) by image processing with the pre-processing method. The image can be used as an input with the algorithm designed so the corresponding output will be achieved according to what's been modeled. With the use of ANN in FPGA, prototyping of blood type classification and identification device was assumed to have an excellent accuracy [5], [6] compare to others [7]–[9].

2. System Design

2.1. Pattern Recognition

Pattern recognition is necessary to determine the type of blood type, define entities, and identify their features. These features are used to distinguish a pattern from others. A good feature is a feature that has a high distinguishing power so that the grouping based on the characteristics they have can be done with optimal accuracy.

The essence of pattern recognition recognizes an object by using various modes, which have a high level of accuracy in the process of recognition. A high degree of accuracy is that an object manually (by humans) cannot be recognized but when using one of the introduced methods of recognition. Some differences in a blood sample after mixed with anti-A and anti-B serum are depicted in Figure 1.

The input systems have been taken from offline pictures captured by a digital Sony DSC w170 (10 MP) camera. There were four image types used, as depicted in Table 1. Resolutions for an image captured are 32x32, 48x48, and 64x64.

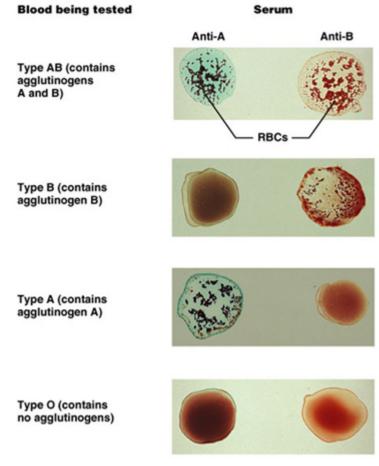


Figure 1 Different Samples of Blood Type After Mixed With Anti A and Anti B Serum

2.2. Training

The training used a backpropagation algorithm to train each blood group to form a pattern or characteristic for each blood group. This scenario is done in MATLAB software, as described in Figure 2.

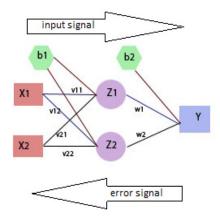


Figure 2 Backpropagation Algorithm for Training Each of Blood Groups

This training aims to know the values of the bits '1' number in each sample as a distinguishing feature. It also obtained the value of final weights used in the design-

forward propagation in FPGA with VHSIC Hardware Description Language (VHDL) as described in Figure 3.

In addition to obtained patterns, the training results are also known to the values of final weights used in testing steps.

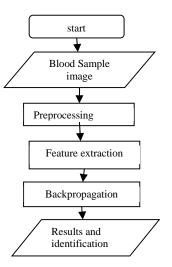


Figure 3 System Flowchart of Blood Cell Type Identification Process Using Backpropagation

2.3. Maintaining the Integrity of the Specifications

At this stage, two tests were conducted, i.e., testing with simulation and testing in implementation. Simulation tests are performed to ensure that the created program can run as designed, while implementation testing aims to ensure that the program can be implemented.

2.4. System Block Diagrams

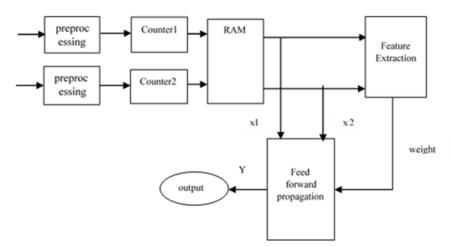


Figure 4 Hardware System Block Diagram for Blood Identification using FF-ANN

We design the hardware implementation using several steps shown in Figure 4. After several simulations for pre-processing and training, we prepared 40 blood image samples for each type with various resolutions, i.e., 32x32, 48x48, 64x64, 80x80, and 96x96 pixels, using MATLAB.

3. Implementation

3.1. RTL Simulation

This simulation is performed on the blocks that make up the ANN implementation on the FPGA to determine the blood type. The purpose of the simulation is to ensure that the program is designed to run in accordance with the desired system, so hopefully, no errors when done implementation on the FPGA. Figure 5 shows the top-level block implemented.

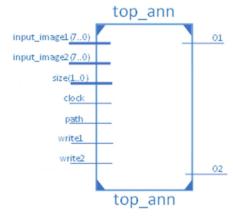


Figure 5 Top Level Block

3.2. Preprocessing

The pre-processing block is the first block that processes the inputs. Inputs of the 8-bit vector are compared to the gray threshold level used. The resulting threshold value is inverted so that the white pixel value should be '1'. Then the value becomes '0'. A similar thing is also done on the pixel value for black. The pre-processing timing diagram simulation shows in Figure 6.

Name	Value	0 us 1 us 2 us 3 us 4 u
⊳ 📑 prein[7:0]	01000100	10001111 00010001 10101000 01000100
🔓 clock	1	
🖓 outpre	1	

Figure 6 Preprocessing simulation results

In the control counter program, there are two programs which consist of counter and memory. The results of the control-counter timing diagram simulation are shown in Figure 7.

lame	Value	500 ns	1,000 ns	1,500 ns	2,000 ns	2,500 ns	1,000 ns	3,
ି clock	•							mir
11 e1	1							
14 e2	1							
្រៀ tulis1	1							
ີ tulis2	1							
🔓 status_transfer	0							
d_out1(12:0)	0000001100001		Q				000000110000	01
d_out2[12:0]	000000110000		X 00	0000000000			000000011000	00
1 reset1	•							
1 reset2	•				-			_
Ug writal	•							4
Writa2	•							4
reada_address1	1 -							
reada_address2	•							_
🏹 ram1_in[12:0]	0000001100010						00000011000	10
🦬 ram2_in[12:0]	000000110001		000	0000000000			000000011000	01
🏹 hasil_1[12:0]	000000000000	000000000000)				00000000000	00
hasil_2[12:0]	000000000000	000	0000000000				00000000000	00
1🔓 n	1101			1101				

Figure 7 Control Counter Simulation Results

The counter program is used to calculate the number of bits '1' from the preprocessing block. The designed counters are used with the incoming images number of inputs to the system.

The memory used is dual input and dual output. The memory's function is to store the calculation results temporarily, and the calculation results will be issued when conditions are met.

3.3. Grouping by Pattern

Name Value 0 us 1 us 2 us 3 us 4 us 5 us is jalan_yuk 1 01 01 01 01 01 01 01 01 01 00011011011 00011001101 00011101101 0001100011001 000110001100 000100011001100 000100011001100 000100110101 0001000110101 0001000110100 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 0001001101010 000100101111000 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 0001001010100 000100100000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 00010000000000 000100000000000 00010000000000 0	X 000100011100 X0. X 000101011011 X0.			
Image: Second state Constraint Constraint <t< th=""><th></th></t<>				
Image: Second and Sec				
Image: bobot_v01[13:0] 0010000000000 UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU	<u>X 000101011011 X0</u>			
bobot_102(13.0) 001000000000 (UUUUUUUUU) X C C010000000000				
▶ W bobot_v11[13:0] 000100000000 (UUUUUUUU	i			
	1			
▶ 📲 bobot_v12[13:0] 000100000000 (UUUUUUUU_)	i			
bobst_v21[13:0] 0001000000000 (UUUUUUUUU)	1 1			
▶ 🖬 bobbt_v22[13:0] 000100000000 (UUUUUUUUU) X 0001000000000	1			
▶ 🖬 bobot_w01[27:0] 0000010010010010 (UUUUUUUU X00000001000000 X000001000000 X00000100100 X00000100000 X000001000000 X00000000	X0000000100000X0.			
▶ 🖬 bbbt_w02[27:0] 0000000100000 (UUUUUUUUX0000010010010X0000010000000X 00000010000000000	X0.			
▶ ₩ bbbt_w11[13:0] 0001010001100 (UUUUUUUUU X 10011011010000 X 000100000000 X 0001010001100 X 10011011010000 X 00010100011000	X 10011011010000 X0.			
bobet_w12[13:0] 1001101101000 (UUUUUUUUUX00010100011000 X000100000000 X 100110110100000	χο.			
▶ w bebet_w21[13:0] 0001010001100 X 0001010001100 X 0001010000 X 000100000000	X 10011011010000 X0.			
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▶ 1 10101 10111 1 X 00001100111 X 0011000100 X 0010000000 X 00100000000	X 001001110111 X0.			
0 X 100101011 X 111011011 X 11101101 X 1110001100	X 100011100 X1.			
0 X 111111011 X 100010100 X 1101010 X 101111100	X 101011011 X1.			
10000000000 0 X 1000000000	1000000000			
▶ ₩ hasil_bagit[11:0] 000000000000 (UUUUUUUUUU X 000000000011 X 000000000001 X 00000000	χ 00000000011 χ0.			
▶ 🚮 hasil_bagi2[11:0] 0000000000011 (UUUUUUUUU X 000000000000 X 00000000000	0000000010			
1001010 0 X 1111111 X 111010101 X 1001010 X 11000 X 11101000	X 10101100 X1.			
11000100 0 X 1010 X 1000100 X 1000110 X 100001000	X 101001010 X1			

Figure 8 Simulation Result of Pattern Grouping

The input that goes into the grouping or pattern selection resulting in a counter bit '1' from the input in the control-counter block. The pattern grouping is based on the ratio of the total number of inputs to the input. The total number of inputs is adjusted to the size of the input image used in the test. Then the pattern obtained will be used to determine the weights corresponding to the pattern. Then the obtained weights used for the forward propagation process to test inputs entered and determine the type of group (A, B, AB, or O) as shown in Figure 8.

3.4. Forward Propagation

Advanced propagation is used in the testing process of the backpropagation algorithm of the final weights obtained in the training process of the input. This process is applied in FPGA in this research.

The output of forwarding propagation is then threshold to simplify the output with 0.5 where the value above 0.5 is '1' and below 0.5 means '0' as shown in Figure 9.

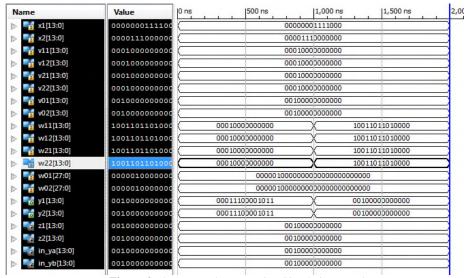


Figure 9 The Forward Propagation Simulation Results

3.5. Hardware Implementation

Xilinx Spartan 3S1000 on XSA-3S Board was used to test our implemented algorithm, as shown in Figure 10. This low-cost board were manufactured by Xess Corp., USA for developing LSI design on FPGA.



Figure 10 XSA 3S1000 From XESS Corp. Showing A Blood Type Result

This board meets our requirements since it uses a Xilinx XC3S1000 chip, complete with XC9572XL CPLD, 32 MByte SDRAM, 2 MByte Flash, and 100 MHz oscillator. It has 4 DIP switches for input and output, 2 pushbuttons, and 7-segment LED. The feed-forward artificial neural network algorithm was synthesized, implement and place based on this FPGA using Xilinx ISE and GXSLOAD software. Targeting this board, we got the system synthesis report as shown in Table 1.

Table 1 FPGA Resource Utilization								
Device Utilization Summary (estimated values)								
Logic Utilization	Used	Available	Utilization					
Number of Slices	746	7680	9%					
Number of Slice Flip	254	15360	1%					
Flops								
Number of 4 input LUTs	1326	15360	8%					
Number of Bonded IOBs	24	173	13%					
Number of MULT 18x18s	8	24	33%					
Number of GCLKs	2	8	25%					

4. Performance Test Results

The test implementation for 40 blood images where each resolution is in accordance with 40 pairs of blood sample images was performed. Based on the test result, based on two parameters, a comparison of resolution with a mean and median number of bit '1' is shown in Figure 11.

As we can see from Figure 11, there are differences in the accuracy of reading the image training in Matlab and FPGA for 32x32, 48x48, 64x64, 80x80, and 96x96 resolutions. Matlab shows that the graphics are constant with an accuracy rate of 92%. Several images are read incorrectly for each resolution. This is because the image's shape has been dripped with the antisera and is not coagulated perfectly. Then, blood droplets and antisera of each image are not measured to each other.



Figure 11 Accuracy Result for Different Image Resolution When Implemented on FPGA Compared with MATLAB Simulation

Whereas in the FPGA, the accuracy has decreased at 80x80 and 96x96 resolutions. This is because the value of comparing the resolution in the FPGA is rounded. This rounding is done because the effect of comma-behind values in the FPGA cannot be read, so rounding is needed.

5. Conclusions

ANN implementation research on FPGA can only be done on the forward propagation of the backpropagation algorithm. This is because of the limitations of the software used to build programs and memory FPGA. Implementation of ANN forward propagation of backpropagation algorithm on FPGA Spartan XSA 3S1000 to determine blood type can be applied with 9% slice requirement, 1% flip flop slice, 4 input LUTs 8%, bounded IOB 13%, MULT18X18s 33%, and GCLKs 25%. The ANN forward propagation test of the backpropagation algorithm on the FPGA to determine the blood type obtained a variety of accuracy performance. Based on the grouping of patterns with the comparison of MATLAB simulation, we obtained an accuracy of FPGA are 92%, 92%, 92%, 90% dan 86% for 32x32, 48x48, 64x64, 80x80, and 96x96 pixel blood image resolutions, respectively. The result of accuracy with a ratio of median value almost equal to the comparison of mean value, accuracy will increase with a magnification of resolution. In the forward propagation algorithm implementation, the test results are highly dependent on the characteristic of the pattern set. If the image resolution used is changed, then the pattern will also change, which affects the output obtained. The value of test accuracy is influenced by the internal factors of the system (pattern determination) and external factors (the absence of rules in the administration of antisera liquid).

6. Future Work

From the results of this research, we plan to develop the products in a real-time system using a low-cost HD camera and internet-based system. We need to develop the system for applied implementation to fulfill the market requirements.

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