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Design and Realization of Digital Modulator BPSK, QPSK and 16-QAM on FPGA

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Abstract

Innovations in the field of wireless communication are growing very rapidly in line with the behavior of modern societies that have high mobility, need of the flexible services, easy access, and high speed data transfer to facilitate any activities of its users. The needs of every user of any variety are more than just voice, video, data transfer, up to a demanding streaming multimedia capabilities and reliability of the communication system used. One of the factors that affect the quality and speed of data transfer in wireless communications is modulation. The development of modulation technology allows data transfer rate to become faster, more resistant to noise, and have high security (encryption) in order to secure data sent over the lead.

The implementation of digital modulator PSK (Phase Shift Keying Modulation) and QAM (Quadrature Amplitude Modulation) on FPGA is designed to simplify the design of a hardware by representing the input which is prepared by using the VHDL programming language. The input will be programmed by logic gates contained in the FPGA into a circuit that functions as a digital modulator. This device can map the input bits into a modulator output that has been mapped in accordance with the coordinates of the constellation.

The expected results of the implementation are three types of digital modulator, namely: BPSK, QPSK and 16-QAM to be implemented on FPGA Xilinx Spartan-6 XC6SLX45 CSG324C; modulation type to be used can be selected by entering input on the programs implemented in the FPGA. In the design used input from laptop devices with UART interface and data types for input is ASCII 8 bit for later analysis simulation results modulation of the input to each modulator using Modelsim for simulation design and Chipscope for simulation system design implemented in the FPGA.

Keywords: BPSK, QPSK, 16-QAM, FPGA, VHDL, UART, ASCII.

1. Introduction

Previous research has discussed the design of the 64-QAM digital modulator on FPGA [4]. In this study we further discuss the design of three types of modulators digital, namely BPSK, QPSK and 16-QAM by using the input configuration of the programming language, i.e. Very High Speed Integrated Circuit (VSIC) and Hardware Description Language (VHDL). This design will be implemented on a single board of FPGA which can then be selected into the type of modulation by tuning the modulator input selector. System modulator will be given by ASCII 8 bit data as the input and the

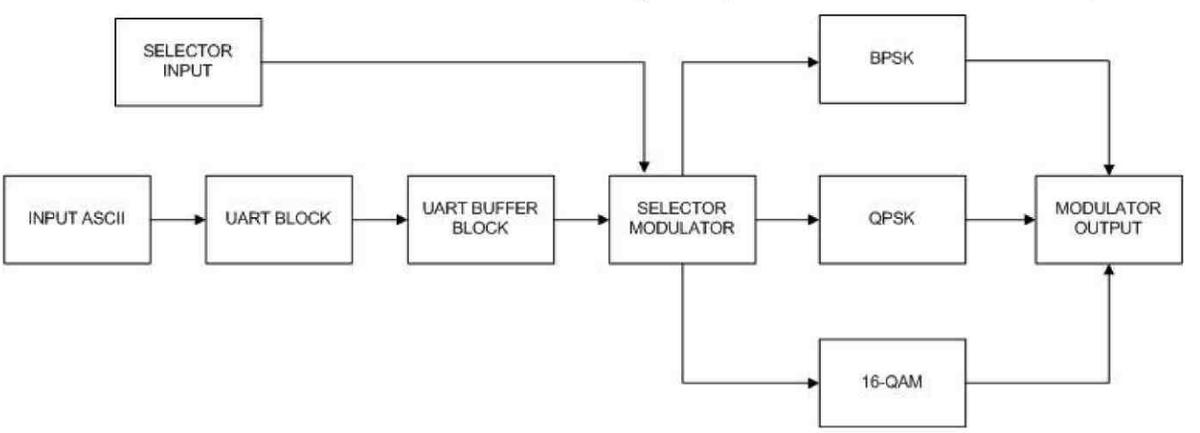

Fig. 1. Modulator System Design Block

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modulated signal will be shown on the Chipscope software. FPGA is used because almost all circuits within the FPGA are integrated in the chip, so the attenuation will be smaller.

2. Sub-system Block Design

2.1 Input Block

The Input Block contains ASCII input from computer device and the UART controller block in the modulator system. The input is the alphanumerical 8-bit ASCII data that are given by computer's keyboard. UART block has a function as an interface between the systems that will be implemented on FPGA devices and computer deiver to give a realtime input to the system. The clock synchronization is required by system to make sure that the input given is correct.

2.2 Buffer Block

Buffer block serves to hold the input of the UART block so that the entering data into the system is the last character that is inserted into the block UART. If the data is given a new input, the entering data is the latest data entered into the system.

2.3 Selector Block

The selector block will select the type of modulator which will be used with certain inputs representing the type of modulator on the system. The input of the system will be passed by the block selector to the modulator selected for use. If the input is "00", so the modulator that will be used is BPSK, "01" for the QPSK modulator and "10" for the 16-QAM modulator. These values are input by changing the Spartan-6 FPGA Switches.

2.4 Modulator Block

Modulator block is a block that contains sub-mapper block, sub-block mixer, sub-block generator sine and cosine generator sub-blocks. The function of Sub-block mapper is to provide a specific value on the input that represents the coordinate value of symbols.

To form a sinusoidal signal at the output of the modulator, the output of sub-block mapper, is multiplied by sine and cosine outputs in which each is for Inphase and Quadrature mapper. The sines and cosines signal are formed by the sine and cosine function generator.

2.5 Modulator Output Block

The function of modulator output block is to display inphase output and quadrature output of each modulator which is only used by a modulator output that will be displayed by a modulator output block.

3. Design and Simulation of Modulator System in VHDL

3.1 Design Modulator System in VHDL

Modulator system will be designed in the VHDL language using the software Xilinx ISE Design Suite 14.5. The design is done by making each block that has been determined in the previous subsection. Subsequently, all blocks that have been made in the form of VHDL are integrated so as to form a system modulator.

3.2 VHDL Modulator System Simulation

The simulations used to see the output of a system have been designed in the VHDL in accordance with the reference [5]. The simulations are carried out to ensure that the modulator block mapper and the shape of the signal generated by the modulator **are** the result of mapping and form of signal modulation in accordance with the results of reference [5]. Simulations are performed on the Modelsim Altera software that can display the form of discrete time signal.

Having seen in the picture if the mapper simulation BPSK modulator input is "0", the coordinates given to the input mapper are (0) in the real / quadrature and (-1) on imag / inphase, when the input is "1", the coordinates given mapper, the inputs are (0) in the real / quadrature and (+1) on the imag / inphase. The simulation result shows that the mapper has been in accordance with the reference [5]. Then it can be seen that the results of mapping results are

Fig. 2. BPSK Mapper Simulation

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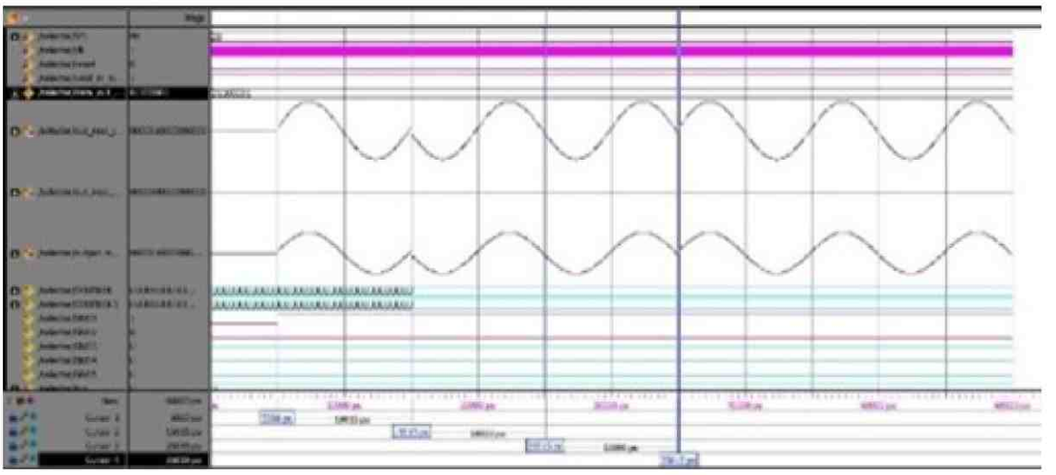

Fig. 3. BPSK Modulator Simulation

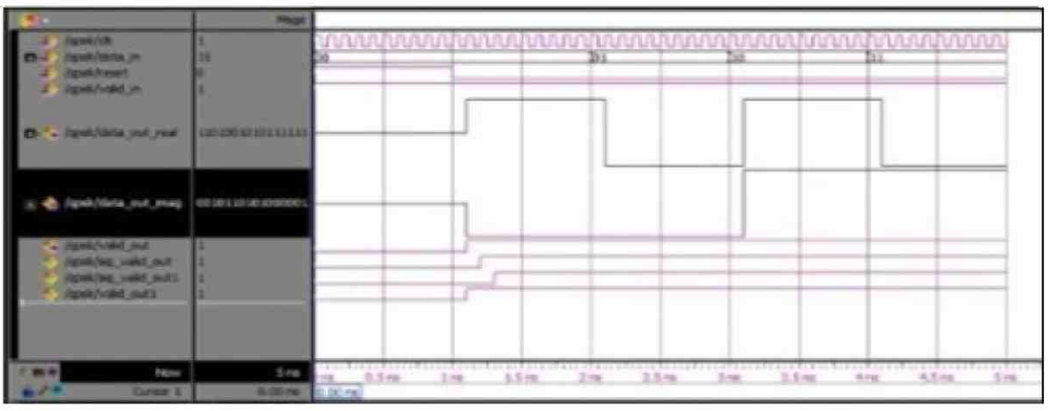

Fig. 4. QPSK Mapper Simulation

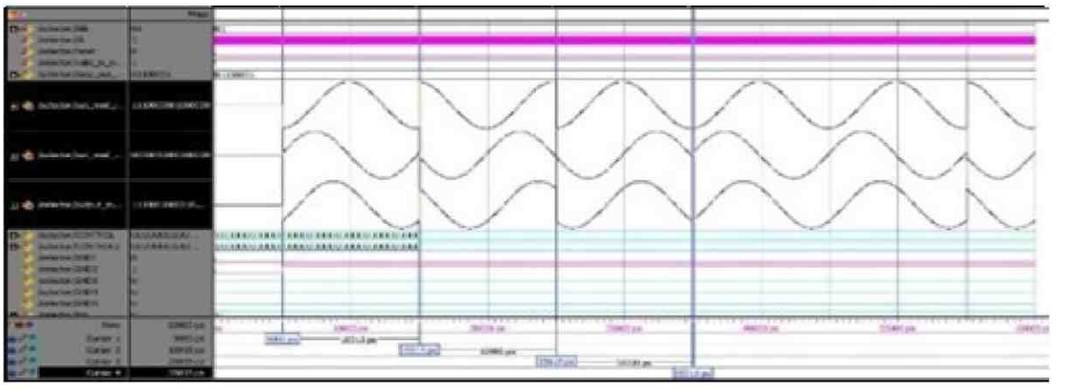

Fig. 5. OPSK Modulator Simulation

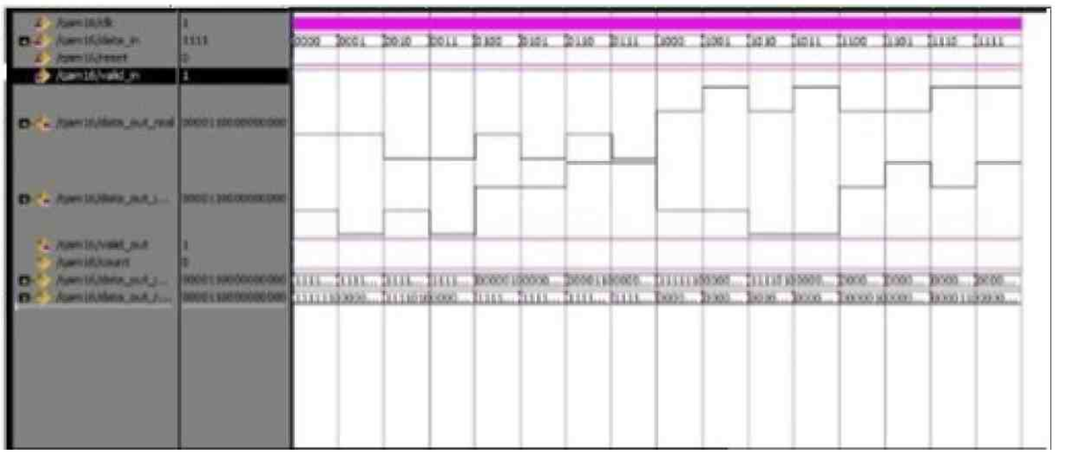

Fig. 6. 16-QAM Mapper Simulation

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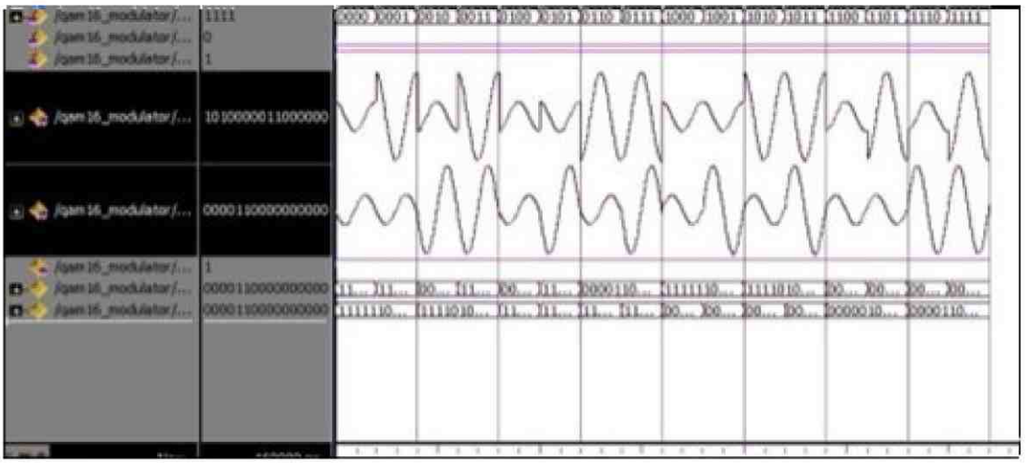

Fig. 7. 16-QAM Modulator Simulation

multiplied signal from the signal generator that generates the sine BPSK signal corresponding to the reference [5] with a large period of each of the full wave of 10.015 nanosecond.

The simulation shows that if the QPSK modulator input is "00" then it gives a real coordinate values (+1) and the imaginary coordinates (-1), if the input is "01" then it gives a real coordinate values (-1) and the imaginary coordinates (-1), if the input is "10" then it gives a real coordinate values (+1) and the imaginary coordinates (+1), and if the input is "11" then it gives a real co ordinate values (-1) and the imaginary coordinates (+1), according to the reference [5]. In the picture visible form of the simulated modulator QPSK modulator output signal has a shape that corresponds with the QPSK signal in the reference [5] and the full wave QPSK signal has a period of 10.015 nanoseconds. Figure 6 shows that the 16-QAM mapper simulation has 4 values for each input. The input sample "0000" gives real coordinate value (-1) and the imaginary coordinate (-1), the input "0001" gives coordinate value (-1) and the imaginary coordinate value (-3). It can be seen that the mapper has been in accordance with the reference [5]. Figure 7 shows the shape of the signal 16-QAM modulation which has 4 levels of different amplitudes and 4 different phases resulted from each different input. The shapes of the output signal modulator 16-QAM are in accordance with the shape of the signal 16-QAM in the reference [5]. The period of one full wave signal 16-QAM is 10.015 nanosecond which is the same as in the BPSK and QPSK modulator.

4. Implemented System Simulation

The simulation is performed after the designed modulator system program has been downloaded to the FPGA board, to provide input from the HyperTerminal application and select the type of modulator by changing the switch port that has been preconfigured so that the switch port is functioning as a modulator selector. The simulation has some input samples which includes character "a" or the 8-bit ASCII codes [01100001], character "m" [01101101] and character "v" [01,110,110].

It is seen in the BPSK modulator output, every one symbol is represented by a single bit of data and forms a sinusoidal wave having a period closer to one symbol period on the simulation results in Modelsim that is equal to 10.015 nanosecond. The form of the output signal modulator implemented on a system that has a shape corresponding to the shape BPSK signal in Modelsim simulation and conforms to the shape BPSK signal [5].

In the QPSK modulator a symbol formed contains two bits of data and one represented wave has a period approaching the period of the symbols on the simulation results in Modelsim. The form of the output signal on the implemented system is in accordance with the shape of the signal FPGA simulation resulted in modelsim and shape of the signal in the reference [5].

In the 16-QAM modulator output symbol formed has the length of 4 bits of data consisting of about 10 nanoseconds as same as in the BPSK and QPSK modulator. The form of the output signal on the implemented system is in accordance with the shape of the signal FPGA simulation resulted in the modelsim and shape of the signal in the reference [5].

From the parameters obtained in the simulation, it can be measured a symbol rate, bit rate, and propagation delay required to produce the symbol signal of each modulator as tabulated in Table 1.

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Table 1. The parameters obtained from simulation

Parameter	Value
Clock	10 ns
Period -Carrier signal (sin & cosine) -*Mapper* BPSK -*Mapper* QPSK -*Mapper* 16-QAM	 100 clock 10,015 *ns* 10,015 *ns* 10,015 *ns*
Quadrature symbol length	16 bit
Inphase symbol length	16 bit
BPSK *Bit rate* QPSK *Bit rate* 16-QAM *Bit rate*	99,85 Mbps 199,7 Mbps 399,4 Mbps

Modulator converts the baseband signal into a passband signal by multiplying the baseband signal output of the carrier signal. The BPSK modulator output consists of one bit per one symbol, the QPSK two bits to one symbol and the 16-QAM four bits per symbol.

From the performed simulation it has been obtained several parameters: a symbol rate, bit rate, and propagation delay. The parameters are obtained from the following equation [10]

$$Rs\ (symbol\ rate) = \frac{1}{Ts} = \frac{1}{symbol\ period} \quad (1)$$

$$R\ (bitrate) = k.Rs\ , k = \frac{bit\ amount}{symbol} \quad (2)$$

$$Bit\ Propagation = \frac{Ts}{k} \quad (3)$$

From the equation it is obtained the symbol rate, the bitrate, and the propagation delay of the BPSK modulator

$$symbol\ rate\ BPSK = \frac{1}{100{,}15\ ns}$$
$$= 99{,}85\ Symbol\ per\ secondbit\ rate\ BPSK$$
$$= \frac{1}{100{,}15\ ns}\ x\ 1$$
$$= 99{,}85\ MbpsBPSK\ propagation\ bit$$
$$= \frac{10{,}015\ ns}{1} = 10{,}015\ ns$$

The same parameters for QPSK modulator is obtained as follows

$$symbol\ rate\ QPSK = \frac{1}{100{,}15\ ns} =$$
$$99{,}85\ Symbol\ per\ secondbit\ rate\ QPSK =$$
$$\frac{1}{100{,}15\ ns}\ x\ 2 =$$
$$199{,}70\ MbpsQPSK\ propagation\ bit = \frac{10{,}015\ ns}{2} =$$
$4{,}933\ ns$And parameters on 16-QAM modulator are as follows.

$$symbol\ rate\ 16QAM = \frac{1}{100{,}15\ ns} =$$
$$99{,}85\ Symbol\ per\ secondbit\ rate\ 16QAM =$$
$$\frac{1}{100{,}15\ ns}\ x\ 399{,}40\ Mbps16QAM\ propagation\ bit =$$
$$\frac{10{,}015\ ns}{4} = 2{,}503\ ns$$**5.**

Conclusions

From the research conducted, it can be concluded that:

a. The systems of digital modulator BPSK, QPSK and 16-QAM modulator along with the selector can be implemented on an FPGA. The implementation results generate 16 bit and 16 bit Quadrature signal in phase signal.

b. The addition of modulator system input with a form of 8-bit ASCII data via UART port on the FPGA, but it needs to be made between the computer interface module and the UART and synchronized so that the input data is right.

c. Based on the results of system simulation and the analysis of the results obtained by implementing the bit rate of 99.85 Mbps BPSK modulators, the modulator of 199.70 Mbps QPSK and the 16-QAM modulator for 399.40 Mbps with a symbol rate for each symbol on each modulator are 99.85 symbols per second. And the propagation delay for each bit is 10.015 nanosecond in the BPSK modulator, 4.933 nanosecond in the QPSK modulator and 2.503 nanoseconds in the 16-QAM modulator.

d. Based on the results of the synthesis of the block system modulator BPSK, the QPSK and 16-QAM found the number of resources needed is a number of slice 199 of the 54 576 available, or 0% of the resource Spartan-6 XC6SLX45-CSG324C, the number of the slice LUT's 398 of 27288 provided or 1% of resource, the number of LUT-FF pairs 177 of the 420 available or 42% of the resource, the number of IOB 40 of the 218 available, or 18% of the resource, the number bufg/BUFGCTRL/BUFHCEs 4 of 16 available or 25% of the resource and the amount DSP48A1s 5 of the 58 available, or 8% of resource. The synthesis of the results, it can be concluded that the results do not exceed the source system implementation on an FPGA so that it can be implemented.

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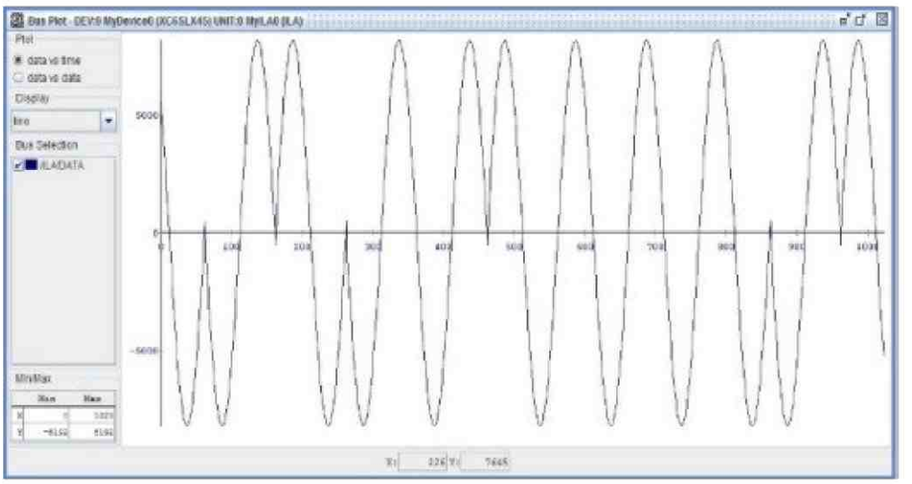

Fig. 8. Inphase output of BPSK modulator with “a” character input

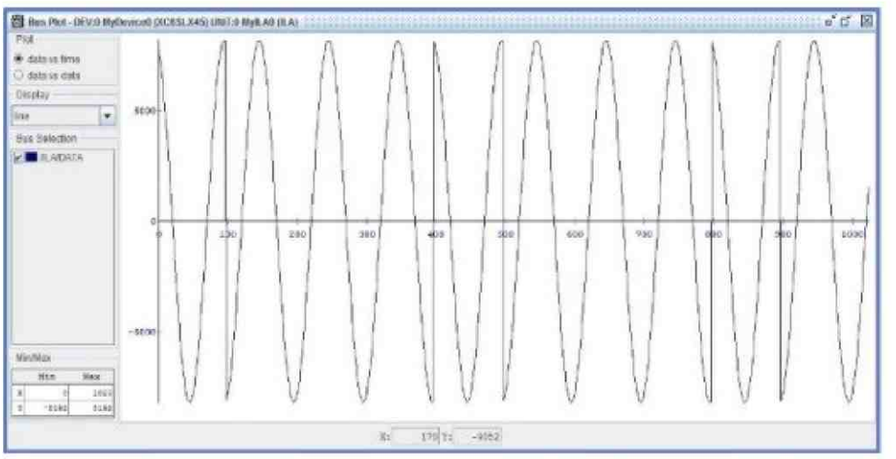

Fig. 9. Inphase output of QPSK modulator with “a” character input

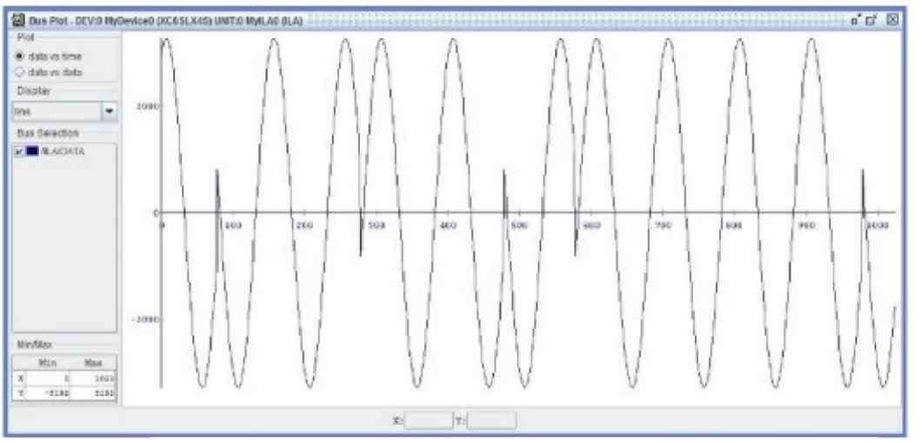

Fig. 10. Quadrature output of QPSK modulator with “a”

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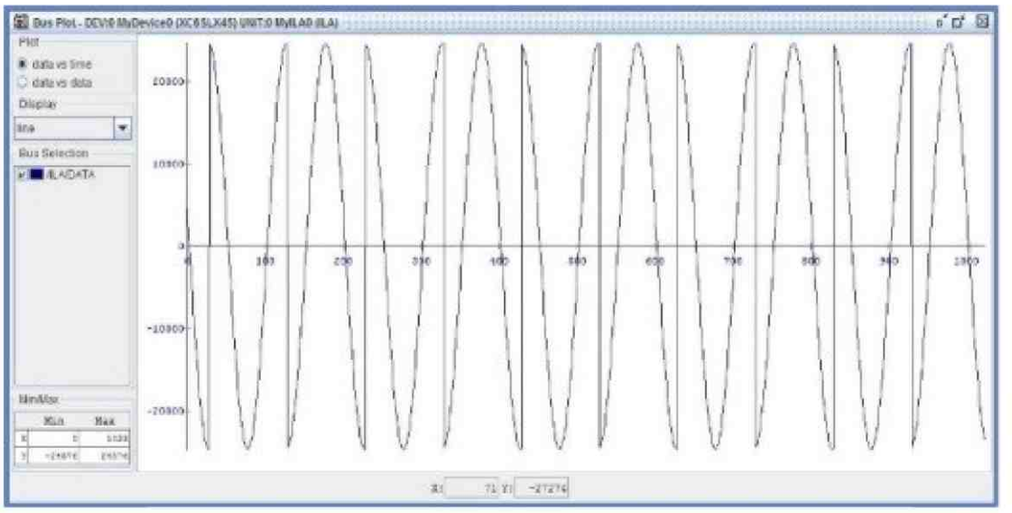

Fig. 11. Inphase output of 16-QAM modulator with “a” character

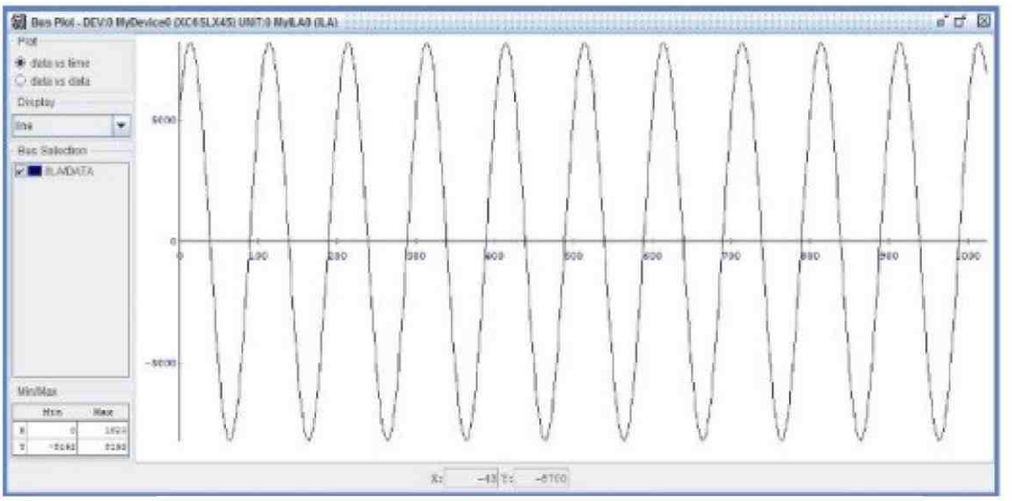

Fig 12. Quadrature output 16-QAM modulator with “a”