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Design and Realization of Memory-Based Chirp Generator on Synthetic Aperture Radar (SAR)

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***Abstract*—Synthetic Aperture Radar (SAR) is a radar system that uses platform movement combined with signal processing. Eventhough it use a small antenna, SAR produce high resolution as good as a large antenna. In SAR imaging, radar is mounted on a moving platform. It transmits electromagnetic pulses and receives backscattered echo signals. Transmitted pulses are subsequently scattered by earth surface and only small portion of them are received by antenna. SAR transmitted signals normally is a chirp or linear frequency modulation (LFM) signal. Chirp signal can be generated by using the analog and digital generator. Digital chirp generator is divided into two methods which are the memory-based and direct digital synthesizer (DDS). The difference of these two methods is located in the memory ROM. In this study, we designed and realized digital chirp generator by using Field Programmable Gate Array (FPGA) DE-1 development board for SAR implementation. It operates in 1.27 GHz (L Band) frequency and had a bandwith of 10 MHz with 24 MHz sampling rate. We found that the output of FPGA is well performed for chirp signal in digital domain.**

Keywords: Digital chirp generator; SAR; Memory-based chirp generator; FPGA;

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1. Introduction

SAR is a radar system that can obtain images with very high resolution by considering its movement with further signal processing. It create a very big 'synthetic aperture' N arrays antenna along its movement resulting a very sharp beamwidth. SAR has proved very useful not only in military surveillance but also for topological mapping and snow monitoring with high resolution. Furthermore, it can operate day and night [1].

SAR implements LFM so that high resolution can be achieved with normal pulse width. LFM or chirp signal can be generated either in analog or digital. Digital chirp generators have advantages such as stability, flexibility, and low cost. It can be change or modified easily by changing the firmware and memory contents of the digital generator [2]. In 2015, analog chirp generator has been designed and realized by Nur Aeni [3] and at same year digital chirp is simulated by Meidwita [4]. In this study we designed 10 MHz bandwidth digital chirp, implemented it in FPGA and converted it to analog by using digital to analog converter (DAC).

2. Design and Implementation

2.1. Digital Chirp

Chirp signal or compressed pulse is a radar pulse with increased or decreased frequency. When the frequency is increased it is called as up-chirp and when the frequency is decreased it is called as down-chirp. The chirp signal equation is expressed in Eq.(1).

$$x(t) = rect\left(\frac{t}{T}\right) Ae^{j\pi\beta t^2} \tag{1}$$

where the function of $rect(x)$ and chirp rate is define in Eq.(2) and Eq.(3) respectively.

$$rect(x) = \begin{cases} 1, & |x| < \frac{1}{2}; \\ 0, & |x| > \frac{1}{2}. \end{cases} \tag{2}$$

$$\beta = \pm\frac{B}{T} \tag{3}$$

The positive and negative signs in Eq.(3) indicate up-chirp and down-chirp, respectively. The amplitude modulation is A and the phase of LFM signal is $e^{j\pi\beta t^2}$ in radians [5] as explained in Eq.(4).

$$\Phi(t) = \pi\beta t^2 \tag{4}$$

The instantaneous frequency $f(t)$ is defined as the derivative of LFM phase as explained in Eq.(5).

$$f(t) = \frac{1}{2\pi}\frac{d\Phi(t)}{dt} = \frac{1}{2\pi}\frac{d(\pi\beta t^2)}{dt} \tag{5}$$

In SAR systems, chirp signals are typicaly modulated over a frequency badwidth range. A sinusoidal signal is generated when the LFM chirp signal is auto-correlated.

In digital chirp generator, the shape of the signal can be configured easily by changing the firmware and the memory content. It is realized by using FPGA which consists of counter IC, memory IC, controller, and DAC. FPGAs is using the Hardware Domain Language (HDL) programming language. In FPGA there is a component called Logic Block which can be programmed according to the will of the user [6]. Generally there are two types of digital chirp generator, which are memory-based and DDS. Memory-based chirp generator stores chirp signal form in memory and repeat it. The repeated signal is a preset signal, therefore the accuracy of the signal is relatively higher than DDS. However it needs to be re-configured for other chirp shapes [7].

2.2. Memory-based Chirp Generator Design

LFM signal is simulated using Matlab as analog signal therefore it need to be converted into digital format. The digital data will be stored in the memory which will be a fidelity on the FPGA [6]. The block diagram of the memory-based chirp generator is shown by Fig.1.

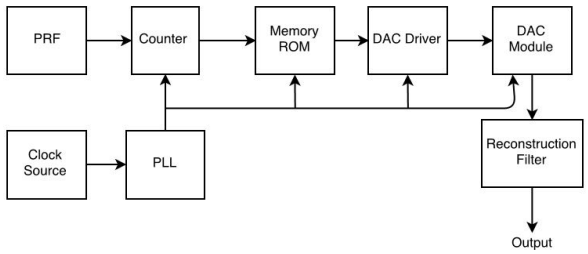

Fig. 1: Memory-based chirp generator block diagram

Binary Counter is a sequential logic which count sequentially from 0 to certain number or until it is ordered to stop. The output of the Binary Counter will be the address of ROM and the data in ROM will be converted to analog signal by using DAC. In this study a digital chirp generator is designed with parameters are shown in Table 1.

Table 1: Chirp design specifications

Parameter	Value
sampling frequency	24 MHz
chirp duration	5 μs
min frequency	0 MHz
max frequency	10 MHz
chirp bandwidth	10 MHz
amplitude	$\pm$ 5V
quantization	8 bit

At first, chirp signals is simulated in Matlab to get the desired output signal as shown in Eq.(6).

$$x(t) = Acos(2\pi f_t t) \tag{6}$$

where

$$f_t = kt + f_0 \tag{7}$$

$$k = \frac{f_t - f_0}{T} \tag{8}$$

A, k, f_0, f_t and T is chirp amplitude, chirp rate, start frequency, end frequency and chirp duration respectively. The equation resulting chirp signal form as shon in Fig.2. The chirp designed with unsigned value therefore the amplitude is 0-2V eventhough in Table 1 stated that it is $\pm$ 5V. However the chirp duration is 5μs as specification and it is represented in 1000 samples.

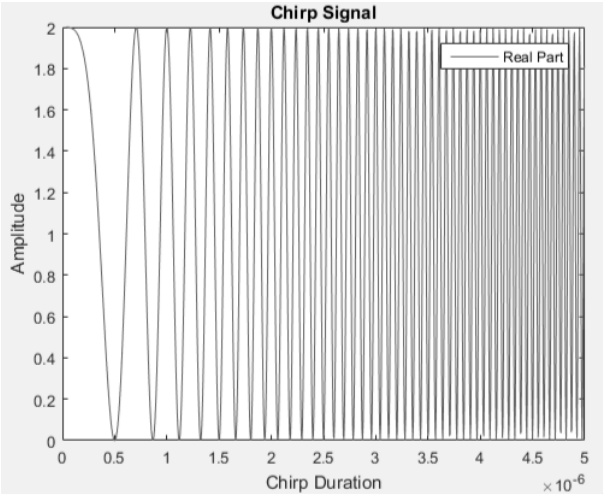

Fig. 2: Chirp signal simulated in Matlab

2.3. FPGA Implementation

Before the output data was implemented in FPGA, it was need to be pre-processed in Altera Quartus II by using VHDL programming language. The output data is in real number and need to be converted to 8 bits binary therefore it can be read in FPGA. The output data was transform to pulses as shown in Fig.3, however for better image resolution it has been cropped to single pulse.

Binary Counter counted from 0-999 to represented 1000 samples and looping. In FPGA implementation, it started with 50MHz input clock and end at 8 pins GPIO which would connected to 8 bits DAC module. We used Altera DE-1 Development and Education Board [8] which detail specification is shown in Table 2.

2.4. DAC Module

By using DAC0808 IC[9], the FPGA output data can be displayed in the osciloscope. It converted 8bits digital data to analog current. It was coupled by TL081 Op-Amp [10] in order to convert current into voltage. The design and realization of DAC module used in this study is shown in Fig.4. Fig.5 shows when it was connected to FPGA board.

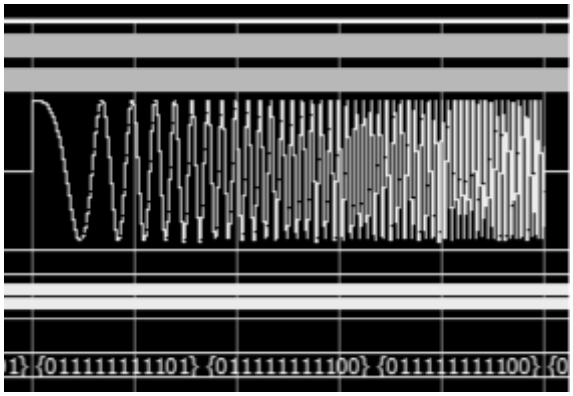

Fig. 3: Chirp signal simulated in Quartus

Table 2: Altera DE-1 specifications

Hardware	**Specifications**
FPGA	Altera Cyclone II 2C20
Memory	512 KB(256K x 16) SRAM 4MB Flash
Clock	50MHz, 24MHz, 27MHz, or external clock sources
I/O	Two 40-pin Expansion Headers
Display	10 red and 8 green LED

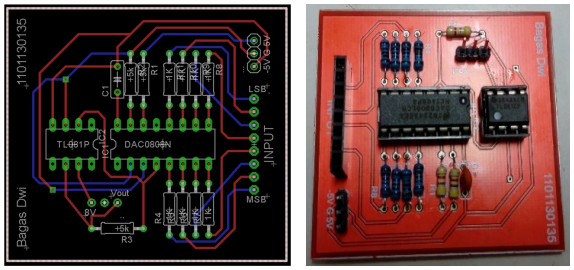

Fig. 4: DAC module

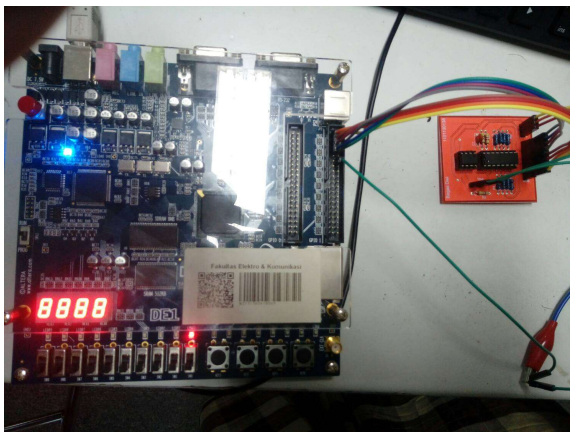

Fig. 5: Digital chirp module

3. Result and Analysis

Parameter measurements on each component of the compiler generator chirp was done to compare between system designed and the realization. The measured components include the DAC module and the result of chirp output signal.

3.1. DAC Module

A comparison between design and realization of DAC module is shown at Table 3. It was measured to obtain the accuracy level. The DAC module have accuracy 85% which maximum error less than $0.03V$. The IC TL081 need to be powered by $8V$ instead of $5V$ at V^+ pin to obtain $5V$ at 11111111 digital input.

Table 3: DAC module comparison

Input A1-A8	V_o Design	V_o Realization
00000000	0V	0V
00000001	19.53mV	16.9mV
00000011	58.59mV	55.5mV
00000111	136.71mV	134.1mV
00001111	292.96mV	291.4mV
00011111	605.46mV	602.2mV
00111111	1.23V	1.23V
01111111	2.48V	2.496V
10000000	2.5V	2.519V
10000001	2.519V	2.538V
10000011	2.558V	2.576V
10000111	2.636V	2.655V
10001111	2.792V	2.812V
10011111	3.1V	3.125V
10111111	3.73V	3.753V
11111111	4.98V	5.02V

3.2. Chirp Signal Verification

The output from DAC module subsequently was connected to oscilloscope resulting analog chirp as shown in Fig.6. The comparison between design and realization is shown at Table.4. The amplitude realization is change to 0-5V instead of $\pm$5V because of DAC0808 can not read signed bits. The sampling frequency is downsized to 6MHz because of DAC0808 settling time is 150ns or maximum frequency sampling supported is 6.67MHz.

Table 4: Comparison between design and realization

Parameter	Design	Realization
f. sampling	24MHz	6MHz
f. range	0-10MHz	0-10MHz
amplitude	$\pm$5V	0-5V
quantization	8bit	8bit

4. Conclusion

From the whole process of design, realization, and measurement of chirp digital generator, it can be concluded that digital chirp generator work as designed with several limitations caused by DAC0808.

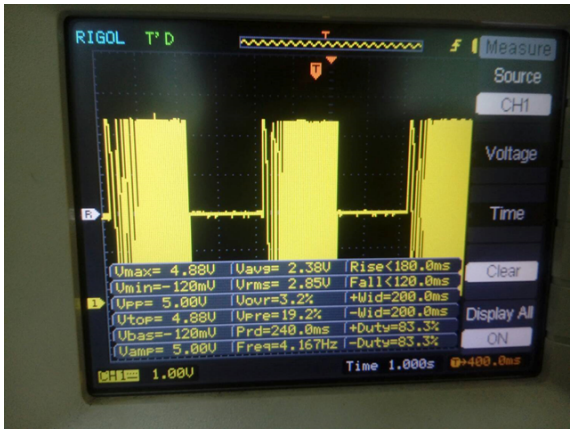

Fig. 6: Digital chirp displayed at oscilloscope

Its frequency sampling limitations and the unability to read signed bits resulting a downgrade in realization of digital chirp. In the future the system need to implement higher specification DAC chip, because Altera Cyclone II FPGA can support output clock up to 50MHz.

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