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Design and Implementation Pulse Compression for S-Band Surveillance Radar in FPGA

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Abstract

The air surveillance radar system consists of four main parts, antenna, RF front-end, radar signal processing, and radar data processing. The S-band radar works in 2.7 GHz to 3.1 GHz. The radar waveform consists of two types of waveform signals, continuous wave (CW) and pulse compression. At the same power transmit level, pulse compression has longer transmission range than CW, because the signal only transmits in short pulse. In the modern radar, waveform is implemented in digital platform. With digital platform, the radar waveform can be optimized without developing the new hardware platform. In this research we have designed and simulated a radar signal processing from baseband to IF using Xilinx ML-605 platform combined with FMC-150 high speed ADC/DAC. Field Programmable Gate Array (FPGA) is the best platform to implemented radar signal processing, because FPGA has ability to work in high speed data rate and parallel processing. The result shows that the implementation of pulse compression radar waveform on ML-605 and FMC150, taped on Chipscope debugger, is matched with Matlab simulation result. With 400 sample of chirp signals, the output matched filter has maximum value on 400th sample, both on simulation and implementation. This research can implement to pulse compression S-band surveillance radar with 2.7 to 3.1 GHz.

Keywords: pulse compression; matched filter; FPGA; ML-605; FMC-150

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1. Introduction

Existing radar system implements full hardware from baseband to radio frequency (RF). This technique is not efficient since one change in the system requirement should be followed by alteration of whole hardware. This process is also time consuming and pricey due to verification process of new design and new hardware development.

Implementing digital signal processing might provide a compact system. It requires few hardware rather than full hardware implementation which needs more space and components to produce radar waveform from baseband to intermediate frequency (IF). Implementation waveform radar using FPGA is more efficient than using hardware, because we can modify the waveform based on different specification without develop the new hardware. It makes efficient on time, dimension and budget. By using FPGA, the system only needs an integrated circuit and few additional components to create similar radar waveform.

Previous works show that the Virtex®-6 FPGA ML605 Evaluation Kit [1] has been used developing system designs that demand high-performance, serial connectivity and advanced memory interfacing. In addition, integrated tools help streamline the creation of elegant solutions to complex design requirements [2].

In this study, we have designed and simulated a radar signal processing from baseband to IF using Xilinx ML-605 platform which combined with FMC-150 high speed ADC/DAC. The FPGA simulation is found to be consistent with the implementation and the resulted waveform can be implemented on S-band.

2. System Modelling

2.1 Radar Signal Processing System

Radar signal processing consist of two parts, they are transmitter (Tx) and receiver (Rx), as in Figure 1. In Tx generator, there are information signal of pulse compression (chirp) in complex number. Chirp signal is in baseband frequency. Chirp signal processed in Digital Up Converter (DUC), to translate chirp signal from baseband frequency to Intermediate Frequency (IF).

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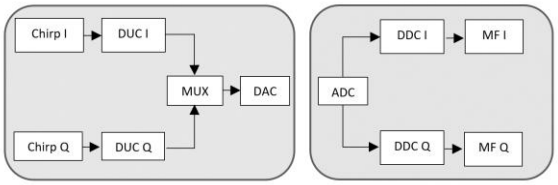


Figure 1: Radar Signal Processing Tx-Rx

In this research the NLFM equation is obtained by mirroring the Linear Frequency Modulation (LFM) signal. Both LFM and NLFM equations are presented in Eq. (1) and (2), respectively, where β is the bandwidth in Hz, t is the timing in second, and τ is the period.

$$x(t) = e^{j\pi\beta t^2/\tau} = e^{j\theta(t)}, 0 \le t \le \tau \quad (1)$$

The NLFM in this research is by mirroring the LFM signal, as in (2).

$$x(t) = e^{j\pi\left(\left(\frac{\beta}{\tau}\right)*\left(t-\frac{\tau}{2}\right)\right)^2} = e^{j\theta(t)}, 0 \le t \le \tau \quad (2)$$

The baseband signal work in 2 MHz of sampling frequency, and the Intermediate Frequency (IF) sampling frequency is 240 MHz. To translate the sampling frequency from 4 MHz to 240 MHz, it needs to implement Digital Up Converter (DUC). DUC consist of up-sampling to increase the sampling frequency from 4 MHz to 240 MHz, and mixer the baseband signal with IF frequency, which is 60 MHz. The IF signal sends through the ADC with minimum sampling 240 MHz.

In the receiver, the IF signal will come from ADC with sampling frequency 240 MHz. In receiver there are two process, Digital Down Converter (DDC) and Matched Filter. The DDC process consist of two process, down conversion from 240 MHz of the IF signal to 4 MHz baseband signal. The output of DDC will process in Matched Filter (MF) to get the receive signal.

The Virtex®-6 FPGA ML605 Evaluation Kit [1] is the Xilinx base platform for developing system designs that demand high-performance, serial connectivity and advanced memory interfacing. This yields design applications for markets such as wired telecommunications, wireless infrastructure, broadcast and many others. Integrated tools help streamline the creation of elegant solutions to complex design requirements [2].

The FMC150 is a dual channel ADC and dual channel DAC FMC daughter card. The card provides two 14-bit A/D channels and two 16-bit D/A channels. [3].

2.2 System Design

The system is designed in Matlab/Simulink with the requirements as in Table 1. There are three main parts on transmitter, developed chirp Inphase (I) and chirp Quadrature (Q), upsampling process, carrier source (sine and cosine waves), mixer, and IQ process, as in Figure 2. On the receiver, there are three main process, mixer, downsampling process, and matched filtering as in Figure 3. The chirp signal is modelling in matlab. To implement in FPGA, the complex signal separate to real (Inphase) and imaginer (Quadrature) part, as in Figure 4.

Table 1. System requirements

Baseband Sampling Frequency	4 MHz
Bandwidth Signal	2 MHz
Pulse Repetition Interval (PRI)	1 ms
Duty Cycle	10% (100 µs)
Chirp Phase	NLFM
IF Sampling Frequency	240 MHz
IF Carrier Frequency	60 MHz

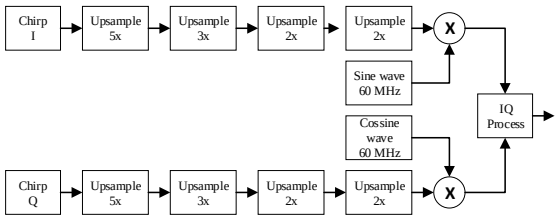


Figure 2: Transmitter

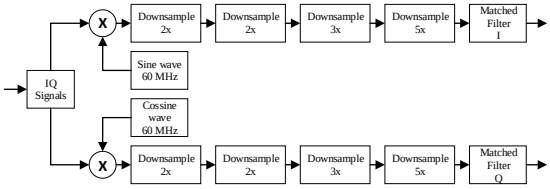


Figure 3: Receiver

The duty cycle of chirp signal is 10%, with one PRI is 1 ms and the baseband sampling frequency is 4 MHz. When transmit signal in one PRI, the sampling frequency is 1 ms = 4000 sample, and 10% from 4000 sample is 400 sample. The transmit chirp is 400 sample in one PRI, as in Figure 5.

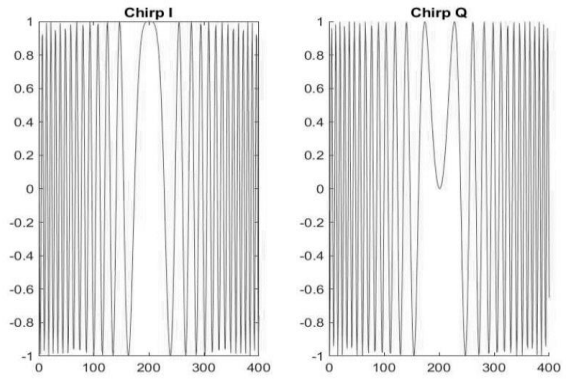


Figure 4: I and Q Baseband Signal

The baseband carrier frequency is 4 MHz, and the IF frequency is 240 MHz. To obtain 240 MHz sampling frequency, the 4 MHz baseband signal need to be multiplied up to 60 times. To void noisy results, this up-conversion process is conducted consecutively by multiplying with 5, 3, 2 and 2 times. The 4 MHz output signal with 240 MHz of sampling frequency, mix with 60 MHz carrier signal with 240 MHz of sampling frequency, as in Figure 6.

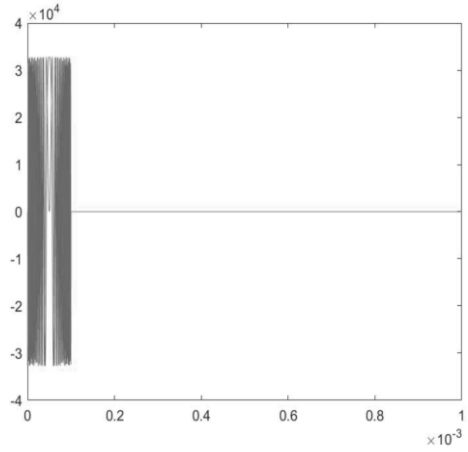


Figure 5: Chirp transmit in one PRI

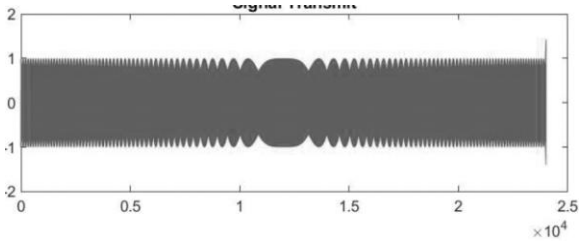


Figure 6: Transmit Signal In IF

Since the baseband signal is separate in I and Q, the carrier in IF is orthogonal signal consist of in-phase (sinus) signals and quadrature (cosine) signals. In the receiver, the input ADC multiply with IF carrier, 60 MHz sinus signals and 60 MHz cosine signals with 240 MHz sampling frequency. The 2 MHz signal with 240 MHz sampling frequency is divided by 5, 3, 2 and 2 times. The 2 MHz baseband signal with 4 MHz sampling frequency is processed in matched filter. The matched filter has filter coefficient which same with the chirp I and chirp Q in transmitter, as in Figure 7.

3. System Implementation

Xilinx ML-605 is development kit for Virtex-6 XC6VLX240T-1FFG1156 FPGA, which have specification as Table 2 [4].

To implement the radar signal processing, ML-605 combined with the FMC-150 high speed ADC/DAC. The FMC150 is a four channel ADC/DAC FMC daughter card. The card provides two 14-bit A/D channels and two 16-bit D/A channels which can be clocked by an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. In addition, there is one trigger input for customized sampling control. The FMC150 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1). The FMC150 has a low-pin count connector, front panel I/O, and can be used in a conduction cooled environment. The ML-605 and FMC-150 show in Figure 8.

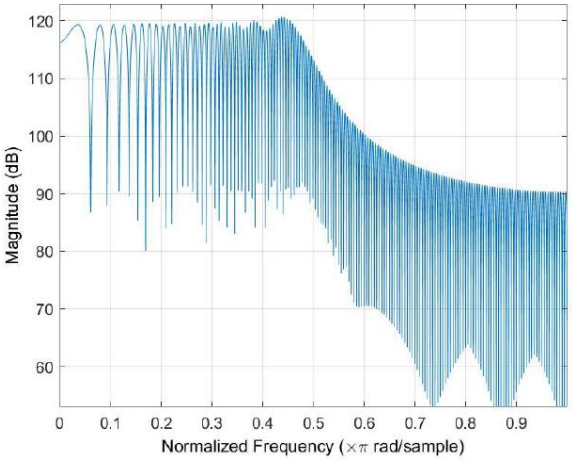
Table 1: Virtex-6 XC6VLX240T-1FFG1156 FPGA Specification

Logic Cells	241,152
Memory (Kb)	14,976
DSP Slices	768
Maximum Transceiver (GTX)	24
Max User I/O	720

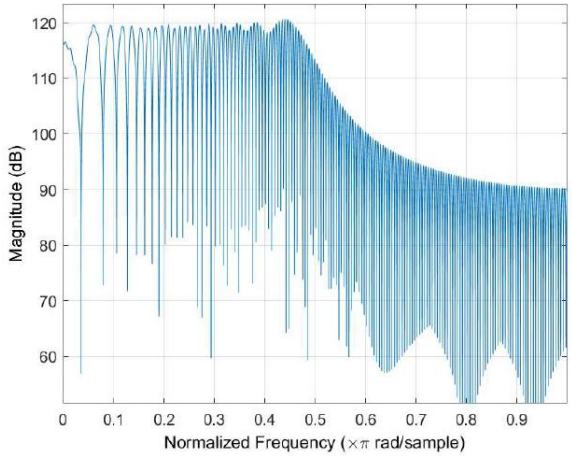
Floating point chirp from Matlab is convert to fixed point lookup table to implement in FPGA. There are two lookup table, chirp I and chirp Q. To validate if the implement signal is according to Matlab simulation, the implementation signal will debug with Chipscope as in Figure 9.

DUC and DDC filter from Matlab produce fixed point coefficient in .coe files. Filter is implement using this coefficient look up table. Sinus and cosinus waves carrier signal lookup table also generated from matlab. To validate if the 60 MHz carrier is correct, the output of FMC150 DAC connected to Spectrum Analyzer, as in Figure 9.

The output DAC connect to the ADC input. The input signal mixed with Inphase (I) and Quadrature (Q) IF carrier signal. Output mixer will process in DDC to translate the sampling frequency from 240 MHz to 4 MHz. The final process in receiver of radar signal processing is matched filter. The matched filter coefficient lookup table generated by Matlab, and the number of coefficients is same with the magnitude of chirp signal in I and Q. The output matched filter I can show in Figure 11, and the output of matched filter Q is show in Figure 12.



7(a)



7(b)

Figure 7(a) Matched Filter I Response Filter and (b) Matched Filter Q Response Filter

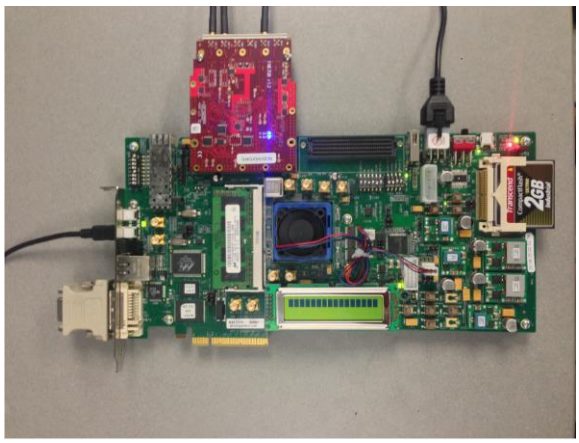


Figure 8: ML-605 and FMC-150

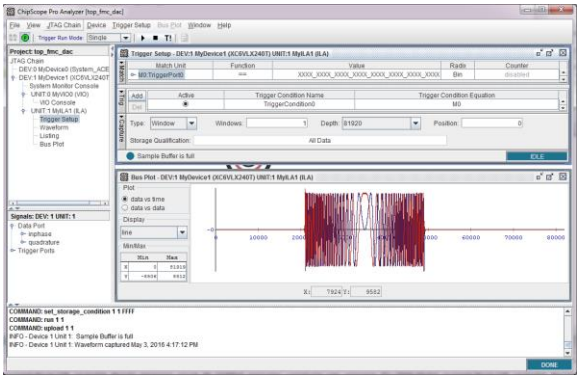


Figure 9: Chirp I and Q implementation in FPGA

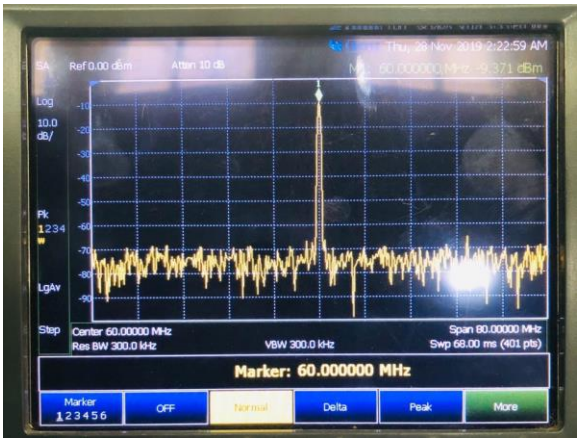
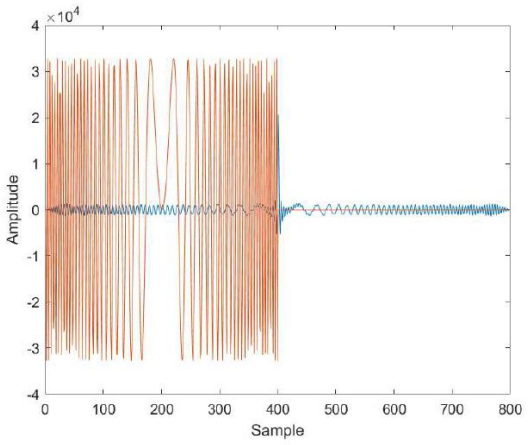


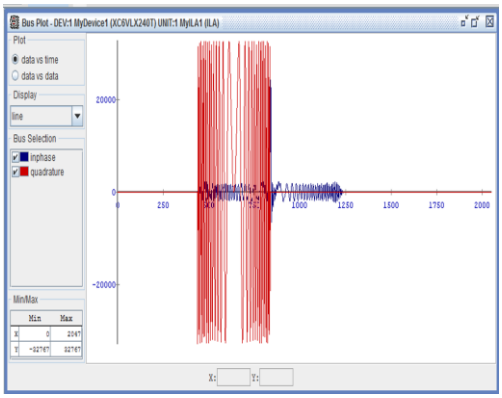
Figure 10: IF carrier signal on Spectrum Analyzer

4. Conclusions

The implementation of pulse compression radar waveform on ML-605 and FMC150, which taped on Chipscope debugger is matched with Matlab simulation. With 400 sample of chirp signals, the output matched filter has maximum value on 400th sample, both on simulation and implementation. This research can be implemented for pulse compression S-band surveillance radar at 2.7 to 3.1 GHz. In the future work, this research can implement in FPGA with add noise, so the SNR can be calculated. The chirp can be changed to smaller duty cycle and calculate the timing process in FPGA.

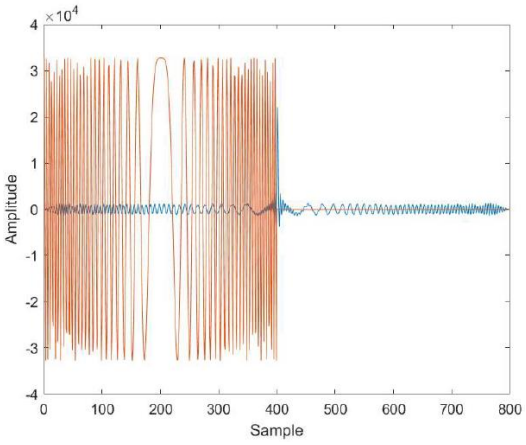


11(a)

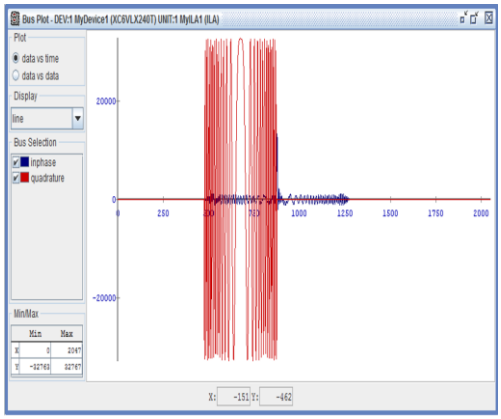


11(b)

Figure 11(a) Chirp (orange line) and Output (blue line) Matched Filter I Matlab Simulation and (b) Chirp and Output Matched Filter I FPGA Implementation on Chipscope.



12(a)



12(b)

Figure 12(a) Chirp (orange lines) and Output (blue lines) Matched Filter Q Matlab Simulation and (b) Chirp and Output Matched Filter Q FPGA Implementation on Chipscope

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